

The figure illustrates a voltage divider circuit used for measuring input resistance. The main circuit consists of a 1MΩ resistor connected to VDD, a 0.1μF capacitor to ground, and a 1kΩ resistor in series with a variable load \$R_L\$. The output voltage \$V_O\$ is measured across \$R_L\$. Below the main circuit, there are two smaller diagrams:

- A simplified model showing a 1kΩ resistor in series with a dependent current source \$\beta I_B\$, where \$I_B\$ is the base current.
- A diagram showing the relationship between \$V_{DD}\$, \$V_{BE}\$, and \$V_O\$.

[illegible]

The diagrams show the pin configurations for the ADXL345 digital accelerometer in four different package types:

- 8-pin DIP:** Pins 1-8 are labeled 1 through 8. Pins 1 and 8 are connected to GND. Pins 2 and 7 are connected to VCC. Pins 3 and 6 are connected to VCC. Pins 4 and 5 are connected to GND.
- 14-pin DIP:** Pins 1-14 are labeled 1 through 14. Pins 1 and 14 are connected to GND. Pins 2 and 13 are connected to VCC. Pins 3 and 12 are connected to VCC. Pins 4 and 11 are connected to GND. Pins 5 and 10 are connected to GND. Pins 6 and 9 are connected to GND. Pins 7 and 8 are connected to GND.
- 16-pin SOIC:** Pins 1-16 are labeled 1 through 16. Pins 1 and 16 are connected to GND. Pins 2 and 15 are connected to VCC. Pins 3 and 14 are connected to VCC. Pins 4 and 13 are connected to GND. Pins 5 and 12 are connected to GND. Pins 6 and 11 are connected to GND. Pins 7 and 10 are connected to GND. Pins 8 and 9 are connected to GND.
- 16-pin QFN:** Pins 1-16 are labeled 1 through 16. Pins 1 and 16 are connected to GND. Pins 2 and 15 are connected to VCC. Pins 3 and 14 are connected to VCC. Pins 4 and 13 are connected to GND. Pins 5 and 12 are connected to GND. Pins 6 and 11 are connected to GND. Pins 7 and 10 are connected to GND. Pins 8 and 9 are connected to GND.

Pinout diagram for the ADXL345 module. The module is connected to a 16-pin header labeled "HEADER XN2" and a 5-pin header labeled "J2".

16-Pin Header Connections:

Pin	Signal
1	GND
2	VCC
3	CS
4	SDA
5	SCL
6	INT
7	VDD
8	GND
9	SDA
10	SCL
11	INT
12	VDD
13	GND
14	SDA
15	SCL
16	INT

5-Pin Header (J2) Connections:

Pin	Signal
1	GND
2	VCC
3	CS
4	SDA
5	SCL

Pin diagram of the 74VHC04 hex inverters. The chip has 14 pins. Pin 1 is labeled '1' and is connected to VCC (5V). Pin 14 is labeled '14' and is connected to GND. Pins 2, 4, 6, 8, 10, and 12 are inputs, labeled '2', '4', '6', '8', '10', and '12' respectively. Pins 3, 5, 7, 9, 11, and 13 are outputs, labeled '3', '5', '7', '9', '11', and '13' respectively. The chip is labeled '74VHC04'.

[illegible]

The left diagram shows a 2-to-1 multiplexer. It has two data inputs, B0 and B1, and one select input, S1. The output is B2. The internal structure shows a 2-to-1 multiplexer with inputs B0 and B1, and select input S1. The output is B2.

The right diagram shows a 2-to-1 multiplexer. It has two data inputs, C0 and C1, and one select input, S2. The output is C2. The internal structure shows a 2-to-1 multiplexer with inputs C0 and C1, and select input S2. The output is C2.