

# CH565W/CH569W Evaluation Board Reference

Version: V1.2

<https://wch-ic.com>

This evaluation board is used for the development of the CH565W/CH569W chips. The IDE uses the MounRiver compiler and can be downloaded for emulation using our official WCH-Link. The CH565/569 is generally referred to as the CH565W or CH569W in the QFN68 package. The CH565M in the QFN40 package lacks the debug interface, eMMC interface, Gigabit Ethernet controller and BUS8 (8-bit active parallel port), a set of SPI and UART, and two sets of PWMX compared to the CH565W.

When users need to use the Gigabit Ethernet and EMMC controller functions of the CH569W, they can also use the CH565W evaluation board by simply replacing the main chip and referring to these instructions.

## 1. Hardware

For the schematic of CH565W evaluation board, please refer to CH565WSCH.pdf.

For the schematic of CH569W evaluation board, please refer to CH569WSCH.pdf.

The following figure shows the descriptions of the CH565W evaluation board.

Figure 1-1 Descriptions of the CH565W evaluation board

Description:

1. Mounting hole	7. DVP supply interface	13. USB 3.0 5Gbps interface	19. VIO selection connector
2. Reserved eMMC Interface	8. SPI flash	14. 5V DC power connector	20. Twisted pair
3. Download serial port U3	9. Download button	15. 3.3V DC-DC switch	21. Gigabit Ethernet PHY
4. DVP interface	10. Reset button	16. 2.5V LDO	22. Optical module
5. Main MCU CH565/569	11. Debug serial port U1	17. Power switch	
6. Debug LED	12. Debug interface	18. Reserved SERDES interface	

CH565W/CH569W is a 32-bit microcontroller based on RISC-V core, with multiple high-speed interfaces. The system clock frequency can be up to 120MHz. It has an internal 16KB 32-bit RAM, a 96KB 128-bit RAM and a 128-bit wide high-speed DMA for data transfer between high-speed interfaces. Compared with CH569W, CH565W provides DVP but lacks HSPI (High-speed parallel interface). CH569W lacks DVP but provides HSPI

(High-speed parallel interface).

The CH565W evaluation board consist of a master MCU (CH565W), USB type A interface, SPI flash, 12-bit DVP, eMMC flash, Gigabit Ethernet PHY chip, optical module, RJ45 UTP network interface (Integrated network transformer), power component and so on. In addition, it also provides UART1 (For routine printf output), UART3 (For ISP download), SPI1 and debug interface. This evaluation board is powerful and resourceful, it can demo almost all functions of CH565W other than PWM output and active parallel port. The PWM output and active parallel port function of CH565W can be demonstrated with the CH569W evaluation board.

The interfaces of some high-speed modules of the CH565W evaluation board share pins with other peripherals, so multiple resistors are used as jumpers. The table below shows alternate function pins of the CH565W evaluation board, alternate peripheral modules, their connection resistors and default functions that users need to pay attention to. When non-default functions are selected, users need to unsolder the default connection resistor and solder the connection resistor of the selected module.

Table 1-1 Alternate function interfaces of CH565W evaluation board and notes

Pinout	Default function and connection resistor	Alternate function and newly added resistor	Notes
PB[18:21]/PA[0:3]	DVP DATA[7:0] R42/R51	eMMC DATA[1:7] R76/R80	R42/R51 and R76/R80 soldered simultaneously may cause signal integrity destroyed
PB[15]	Hardware reset input RST# connected directly	Ethernet PHY interrupt input R36 DVP data line[10] Network resistor R41	RST enabled/disabled by ISP tool; RST, PHY interrupt input and DVP data input cannot be enabled simultaneously
PB[3:4]	RGMII_TXD[2:1] connected directly	UART3 R87/R86	R87/R86 soldered may cause RGMII interface signal integrity destroyed
PB[11:14]	RGMII_RXD[0:1]/ RGMII_RXDV eMMC_CLK1 connected directly	SPI1_SCS SPI1_SCK SPI1_MOSI SPI1_MISO R22/R21/R20/R34	Unless SPI1 is necessary, do not solder R22/R21/R20/R34
RGMII_RXD1	UTP twisted pair mode R46	Fiber mode R45	Please refer to the user manual for Ethernet PHY related configurations.

*Note: When the Ethernet function and the supporting physical layer chip are in use, due to the particularity of the Ethernet function, a large number of configuration resistors are used to configure the MDI side type, MII side type, MII interface level, TXC clock source of the MAC side of the Ethernet physical layer and other configuration information. The Ethernet module of the CH565W evaluation board is configured to be in the most commonly used mode when leaving the factory, that is, the MDI side uses UTP twisted pair, and the MII level is set to 3.3V, etc. If the user wants to modify the above parameters, please refer to the manufacturer datasheet of the physical*

layer and the document of the Ethernet driver routine provided by us, or directly call us for technical support of our network product line.

The following figure shows the descriptions of the CH569W evaluation board.

Figure 1-2 Descriptions of the CH569W evaluation board

Description:

- |                      |                           |                         |
|----------------------|---------------------------|-------------------------|
| 1. Main control MCU  | 5. HSPI interface         | 9. Type-C interface     |
| 2. Voltage regulator | 6. Serial port 1          | 10. DC supply connector |
| 3. Voltage regulator | 7. ISP download interface | 11. SERDES interface    |
| 4. SPI FLASH         | 8. USB3.0 interface       | 12. LED                 |

The CH569W evaluation board consist of a master MCU (CH569W), USB type A interface, DC supply connector (5mm), USB Type-C interface (Only used to supply power), SPI flash, power component and so on. In addition, it also provides HSPI interface (High-speed parallel interface), SERDES interface, UART1 (For routine printf output), UART3 (For ISP download), and ISP download interface. This evaluation board is powerful and resourceful.

The HSPI interface of the CH569W evaluation board share pins with other peripherals, so some resistors are used as jumpers. The table below shows alternate function pins of the CH569W evaluation board, alternate peripheral modules, their connection resistors and default functions that users need to pay attention to. When non-default functions are selected, users need to unsolder the default connection resistor and solder the connection resistor of the selected module.

Table 1-2 Alternate function interfaces of CH569W evaluation board and notes

Pinout	Default function and connection resistor	Alternate function and newly added resistor	Notes
PB[11:15]	HSPI R2/R22/R33	ISP download function R1/R21/R30	R2/R22/R33 and R1/R21/R30 should not be soldered simultaneously

*Note: There are two cases for HSPI, choose the upper board or the lower board according to the different resistors soldered. Solder R32/R33 on the upper board, or solder R34/R35 on the lower board. R32/R33 and R34/R35 should not be soldered simultaneously.*

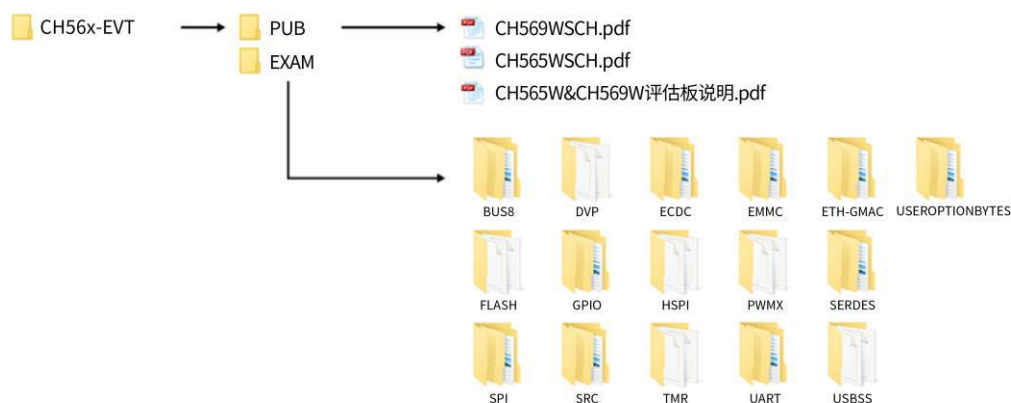
## 2. Software

Please download CH569EVT.ZIP file from our website, which contains the routines of CH565 interfaces. the routines of CH565 and CH569 are common, but CH565 doesn't include HSPI interface.

For the structure of CH569EVT.ZIP, please refer to the CH569\_List.txt document.

Open the EXAM folder to see the related routines of CH565. Categorized by peripherals and functions, the structure of CH565 routines is distributed as shown in the figure.

Figure 2-1 Routine Structure Distribution of CH565



Among them, SRC is the chip project public file, and the rest are the demo files of each peripheral. The demo files of each peripheral have been created IDE project, users can refer to use.

The CH565/CH569 are developed using the Mounriver IDE. You can download the Mounriver IDE from our website. Mounriver has a built-in *MounRiver Studio Help Manual*, which you can follow to install, import and create new projects.

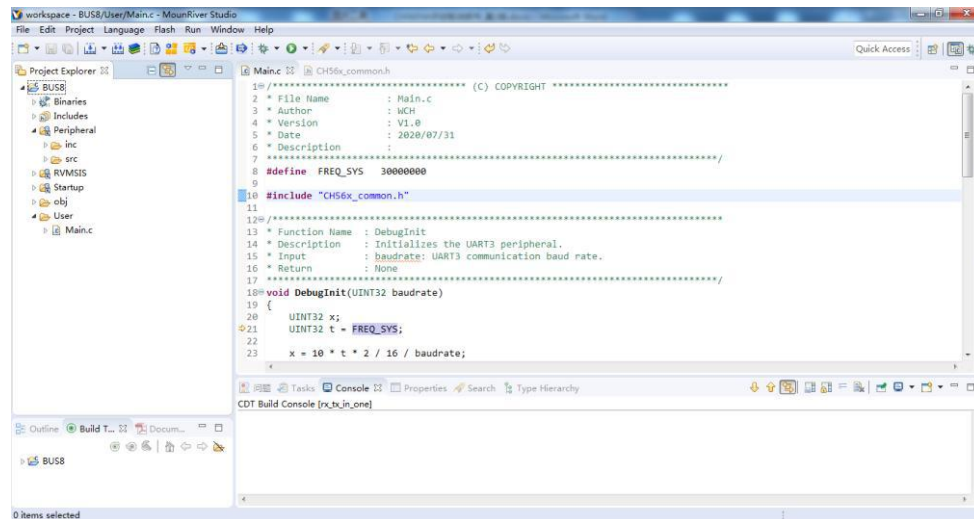
### 2.1 Open Project / Import Project

The user can tap any peripheral project, for example, tap the eight-bit bus routine "BUS8".

Figure 2-2 Layout of files in BUS8 folders

Click on one of the BUS8.wvproj files to bring up MounRiver Studio and open the corresponding project.

Figure 2-3 Wakeup mounriver display after opening USBHS.wvproj

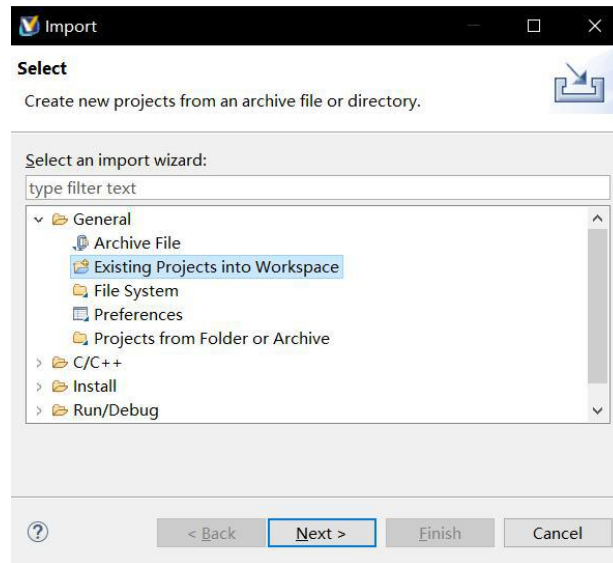


In addition, you can also open existing projects by importing them. Open Moonriver, right-click in the blank space of the ProjectExplorer interface on the left, and select import from the pop-up menu, as shown in Figure 2-4.

Figure 2-4 Open the import menu

Select an existing project in the pop-up menu.

Figure 2-5 Select to open an existing project



Select the directory containing the project files.

Figure 2-6 Select project directory

This operation can also open the project.

## 2.2 Compilation

Figure 2-7 USBSS engineering interface

In the figure, 1 is incremental compilation, which only compiles the modified parts, and the compilation speed is fast. 2 is rebuild, which is global compilation of the selected project, and the speed is slower. Select rebuild here, and the compilation result is as shown in the figure.

The default compilation will generate an executable .hex file. We need to download the hex file to the evaluation version to run. Note that MounRiver compilation settings such as project file directory, linker, and optimization level are explained in the "MounRiver Studio Help Manual".

## 2.3 Download

Please download the WCHISPTool.exe tool from our official website to download the hex file to the chip flash operation.

The CH565W chip needs to enter download mode in order to use the ISP tool to download the code, it is generally most convenient to use the USB method to download the code, the CH565W chip will enter the download mode when it detects the following two conditions at power on, one is to detect the first 16 bytes of flash as 0xff, the second is to detect the boot pin is at low level. If the chip does not communicate with the ISP tool within 10 seconds after entering the download mode, it will automatically exit the download mode.

Connect the CH565W evaluation board to the computer using the USB plug to plug cable. Open our official ISP download tool, select CH565/CH569 as the chip signal, select USB as the download method, power off the CH565W evaluation board, then press and hold the download button on the board and power on again. Check the "Run target program after download" and "Enable RST pin as manual reset input pin" as required, select the .hex file generated in 2.2 in the user program file field, and finally click "Download", the program in 2.2 can be downloaded to the main chip on the evaluation board and run automatically.

To download code to the CH565/569 evaluation board using the serial port, connect the TXD and RXD pins of the chip UART3 to the computer via the USB to TTL module (If using the CH565 evaluation board you will also need to solder a 0Ω resistor on the back of the R86/R87 to ensure the serial port is connected), press and hold the download button or ground the download configuration pin (Factory default PA5) and then power on the evaluation board. The evaluation board will be powered on, open the WCHISPTool tool, select the chip model at 1, select the download method for the serial port at 2, click search at 5, select the port number connected to the evaluation board, and finally click download at 6 to start the code download operation, the download record will show the specific steps and status, the serial download time varies with the size of the code from a few seconds to

more than ten seconds.

Figure 2-8 Use ISP tool to download code



### 3. Contact Us

If you have any questions related to using the CH565W/CH569W evaluation board, please send a description of your problem to: [tech@wch.cn](mailto:tech@wch.cn) or call Technical Support phone number on our website.