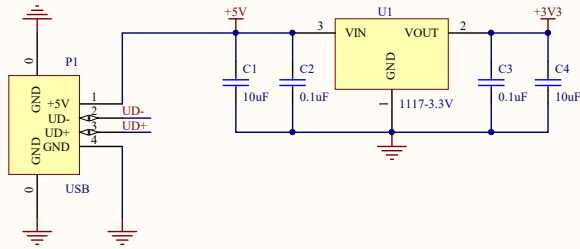
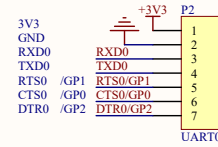


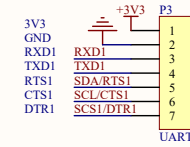
POWER



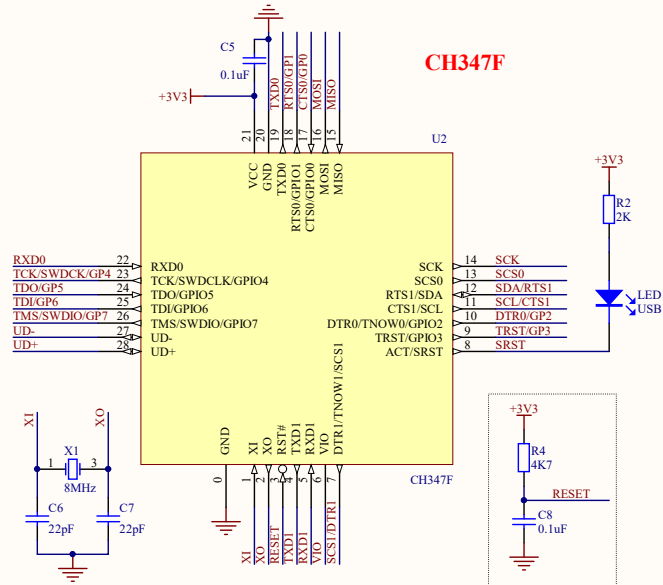
UART0



UART1



CH347F

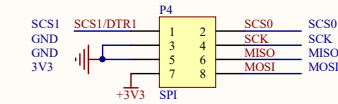


This reset circuit is designed as optional

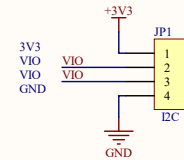
FLASH_CS



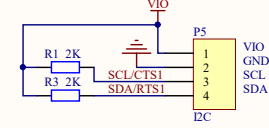
SPI



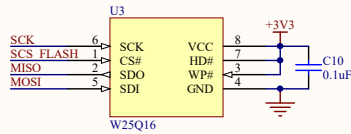
VIO



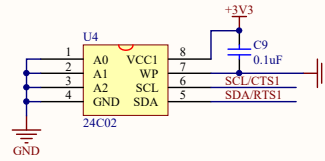
I2C



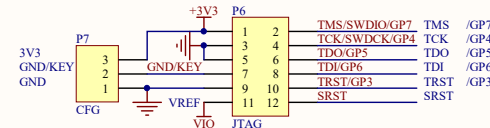
SPI FLASH



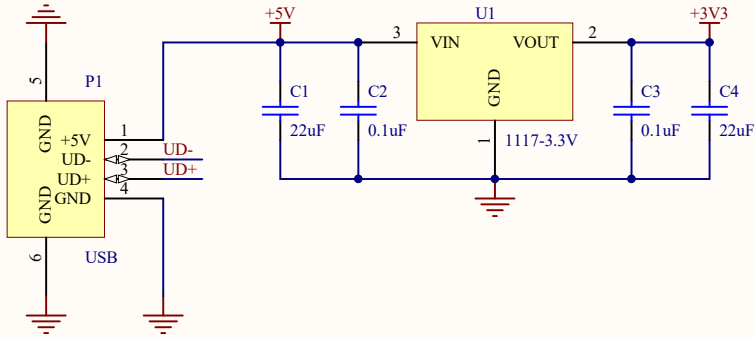
EEPROM



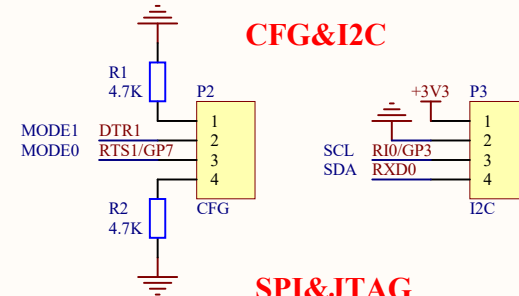
JTAG



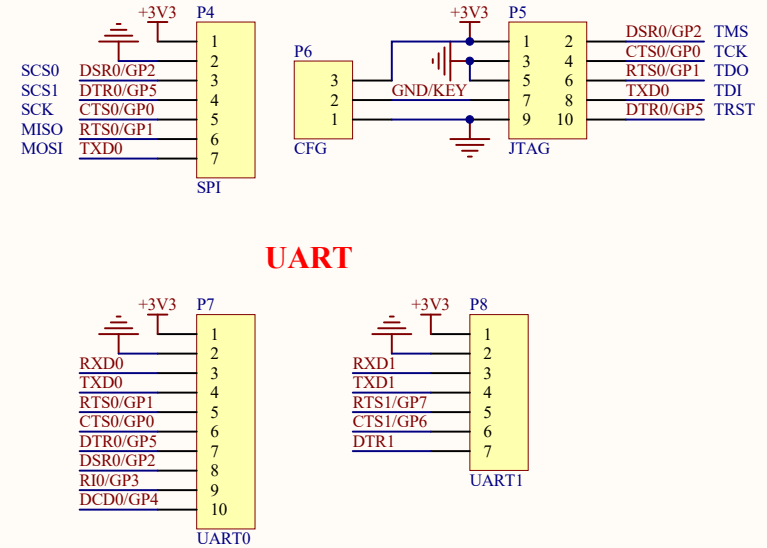
POWER



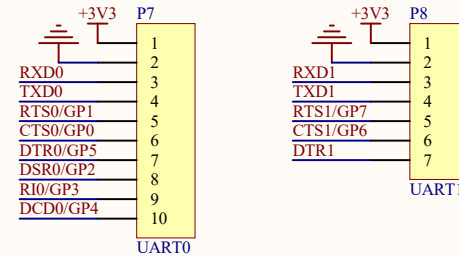
CFG&I2C



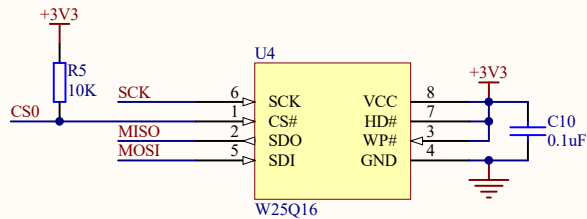
SPI&JTAG



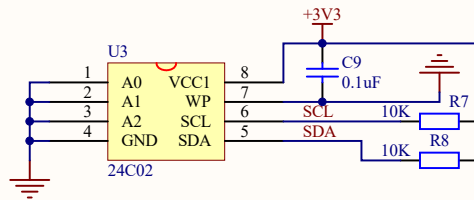
UART



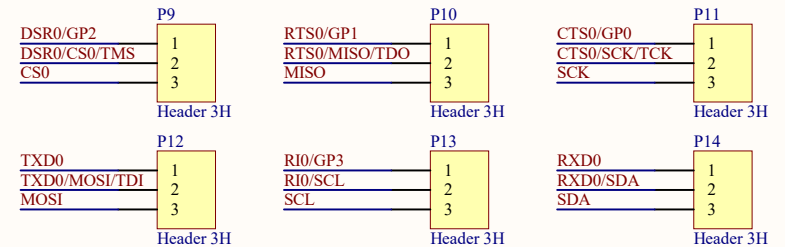
SPI FLASH



EEPROM



IO SWITCH



This reset circuit is designed as optional

