

High-speed USB Converter Chip CH347 Evaluation Board Description and Application Reference

1. Introduction

CH347 evaluation board is used to demonstrate interface functions of 480Mbps high-speed USB convert chip CH347 for USB to UART/HID, USB to UART/ SPI/I2C/JTAG/GPIO, programming of EEPROM and FLASH. CH347 has built-in EEPROM. Configure parameters such as VID, PID, vendor and product information string, etc. can be configured by software CH34xSercfg.exe.

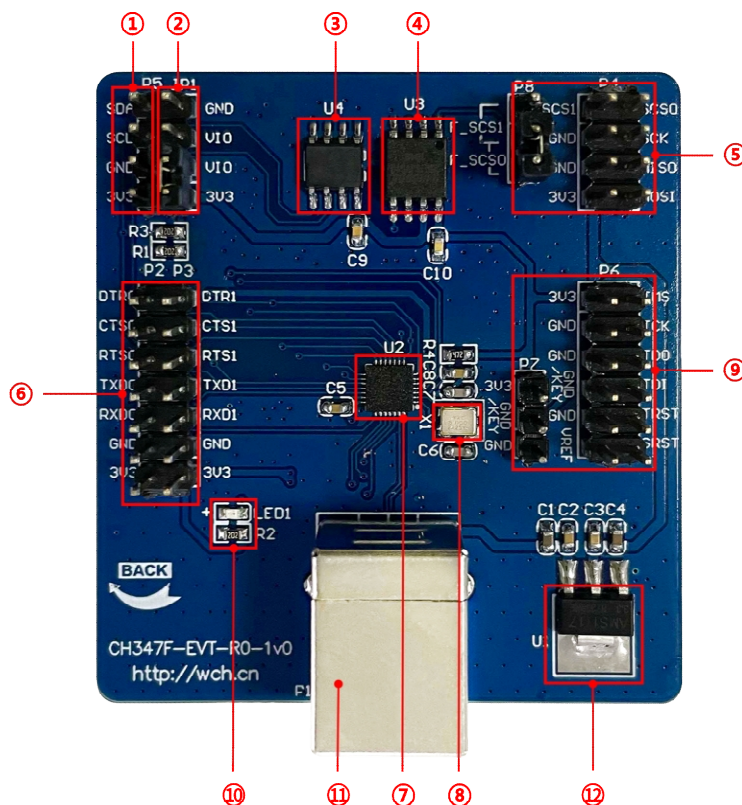
USB to UART of CH347 used to upgrade directly from normal serial product to USB 2.0. CH347 provides two high-speed UART which supports controlling RS485 to transmit-receive switch, hardware flow control, and common MODEM communication signals. USB to SPI interface (SCS line, SCK/CLK line, MISO/SDI/DIN line, MOSI/SDO/DOUT line) can be used to control a variety of SPI-compatible devices or communicate with FPGA and other devices in high rate (up to 60MHz), USB to JTAG interface (TMS, TCK, TDI, TDO and TRST) can be used to operate CPU, DSP, FPGA, CPLD and other devices to achieve debug and download functions (up to 60MHz), USB to GPIO function can be used for simple digital I/O control. USB to I2C synchronous serial port (SCL line, SDA line) can be used to control various I2C compatible devices, such as serial EEPROM.

2. Evaluation board hardware

2.1. CH347F high-speed USB to JTAG&SWD&SPI&I2C&UART

Refer to CH347SCH.pdf document for evaluation board design.

The physical picture of the evaluation board is shown below:



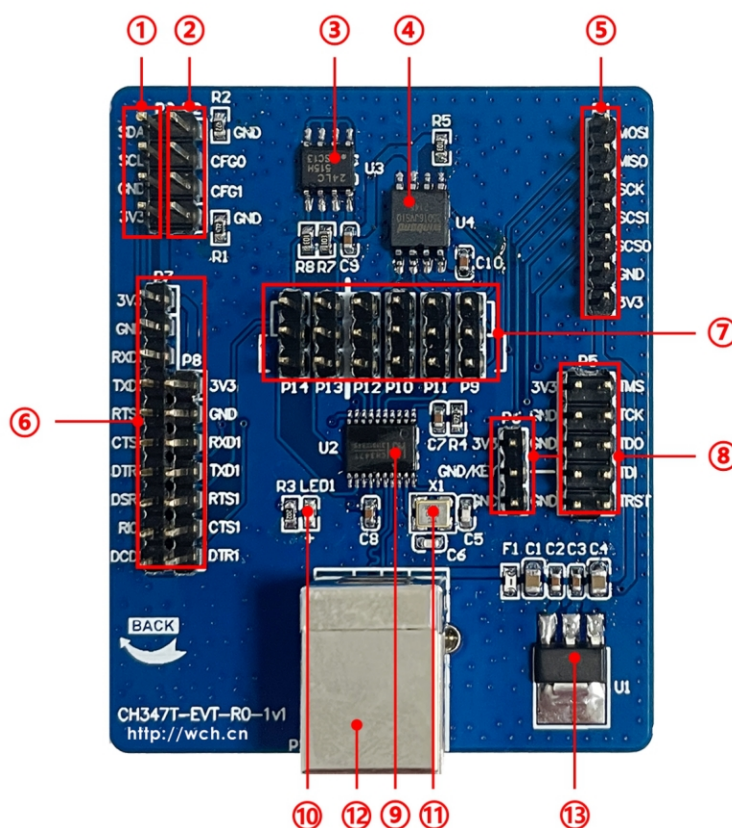
Function description of each unit:

- ①: P5-I2C communication interface, led out by pin header
- ②: VIO power supply selection interface, IO voltage is 3.3V when VIO is shorted to 3V3
- ③: EEPROM device 24C02, CH347F can operate this device directly
- ④: FLASH device 25Q16, CH347F can operate this device directly
- ⑤: P8- FLASH device chip selection, P4-SPI communication interface, led out by pin header
- ⑥: TTL UART0/1, led out by pin header
- ⑦: U2- Master controller chip CH347F
- ⑧: Passive crystal oscillator with 8MHz frequency
- ⑨: P6, P7-JTAG/SWD communication interface, led out by pin header
- ⑩: LED1-ACT pin indicator LED, indicates USB configuration completion status
- ⑪: P1-USB interface, connects to USB host via USB cable
- ⑫: U1-3.3Vvoltage conversion chip, converting VBUS of USB interface to 3.3V for the master chip power supply, it can also be designed to use an external 3.3V power supply directly to power CH347F and peripherals

2.2. CH347T high-speed USB to JTAG&SWD&SPI&I2C&UART

Refer to CH347SCH.pdf document for evaluation board design.

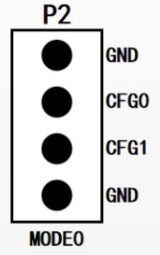
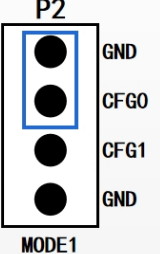
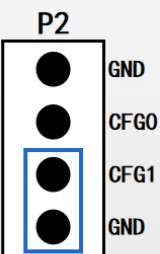
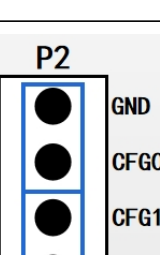
The physical picture of the evaluation board is shown below:



Function description of each unit:

①: P3-I2C communication interface, led out by pin header

②: CH347T switch pin of working mode (pin level is high in suspended state)

Mode	Mode Description	CFG0	CFG1	Evaluation board wiring diagram
Mode 0	USB to dual high-speed UART	1	1	
Mode 1	USB to single high-speed UART (VCP) + SPI + I2C	0	1	
Mode 2	USB to single high-speed UART (HID) + SPI + I2C	1	0	
Mode 3	USB to single high-speed UART (VCP) + JTAG/SWD	0	0	

③: EEPROM device 24C02, CH347T can operate this device in working mode 1/2

④: FLASH device 25Q16, CH347T can operate this device in working mode 1/2

⑤: P4-SPI communication interface, let out by pin header

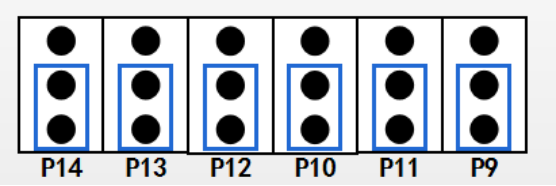
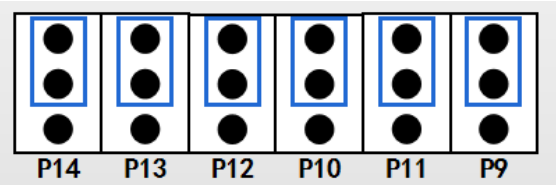
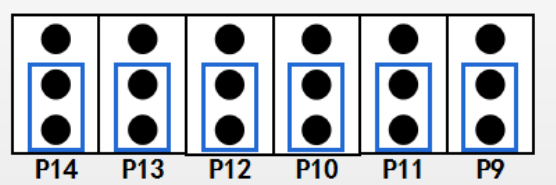
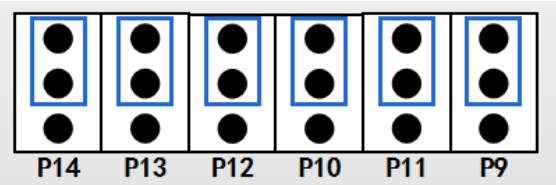
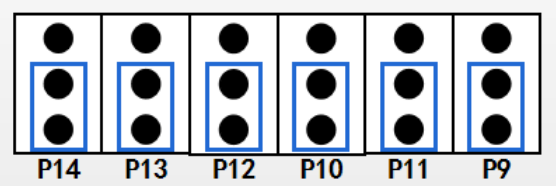
⑥: TTL UART 0/1, led out by pin header, Mode 0: supports UART0 and UART1

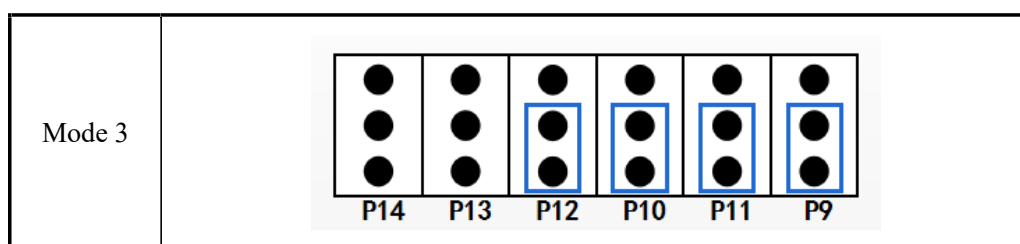
Mode 1/2/3: supports only UART1

⑦: P9-P14 functional pin configuration area

Pin Header	P14	P13	P12	P10	P11	P9
1	SDA	SCL	MOSI	MISO	SCK	CS0
2	RXD0/SDA	RI0/ SCL	TXD0/MOSI/ TDI	RTS0/MISO/ TDO	CTS0/SCK/ TCK	DSR0/CS0/ TMS
3	RXD0	RI0/ GP3	TXD0	RTS0/GP1	CTS00/GP0	DSR0/GP2

Pin configuration connections in different modes

MODE	Pin area configuration (Unmarked areas of the pins can be left unconnected.)
Mode 0	 <p>P14 P13 P12 P10 P11 P9</p>
Mode 1	 <p>P14 P13 P12 P10 P11 P9</p> <p>Operate the EEPROM and FLASH on the board</p>  <p>P14 P13 P12 P10 P11 P9</p> <p>Use SPI+I2C interface</p>
Mode 2	 <p>P14 P13 P12 P10 P11 P9</p> <p>Operate the EEPROM or FLASH on the board</p>  <p>P14 P13 P12 P10 P11 P9</p> <p>Use SPI+I2C interface</p>



⑧: P5, P6-JTAG communication interface, by pin header out

⑨: Master controller chip CH347T

⑩: LED1-ACT pin indicator, indicates the USB configuration status

⑪: Passive crystal oscillator with 8MHz frequency

⑫: P1-USB interface, connected to USB host via USB data cable

⑬: U1-3.3V voltage conversion chip, converting VBUS of USB interface to 3.3V for the master chip power supply, it can also be designed to use an external 3.3V power supply directly to power CH347T and peripherals.

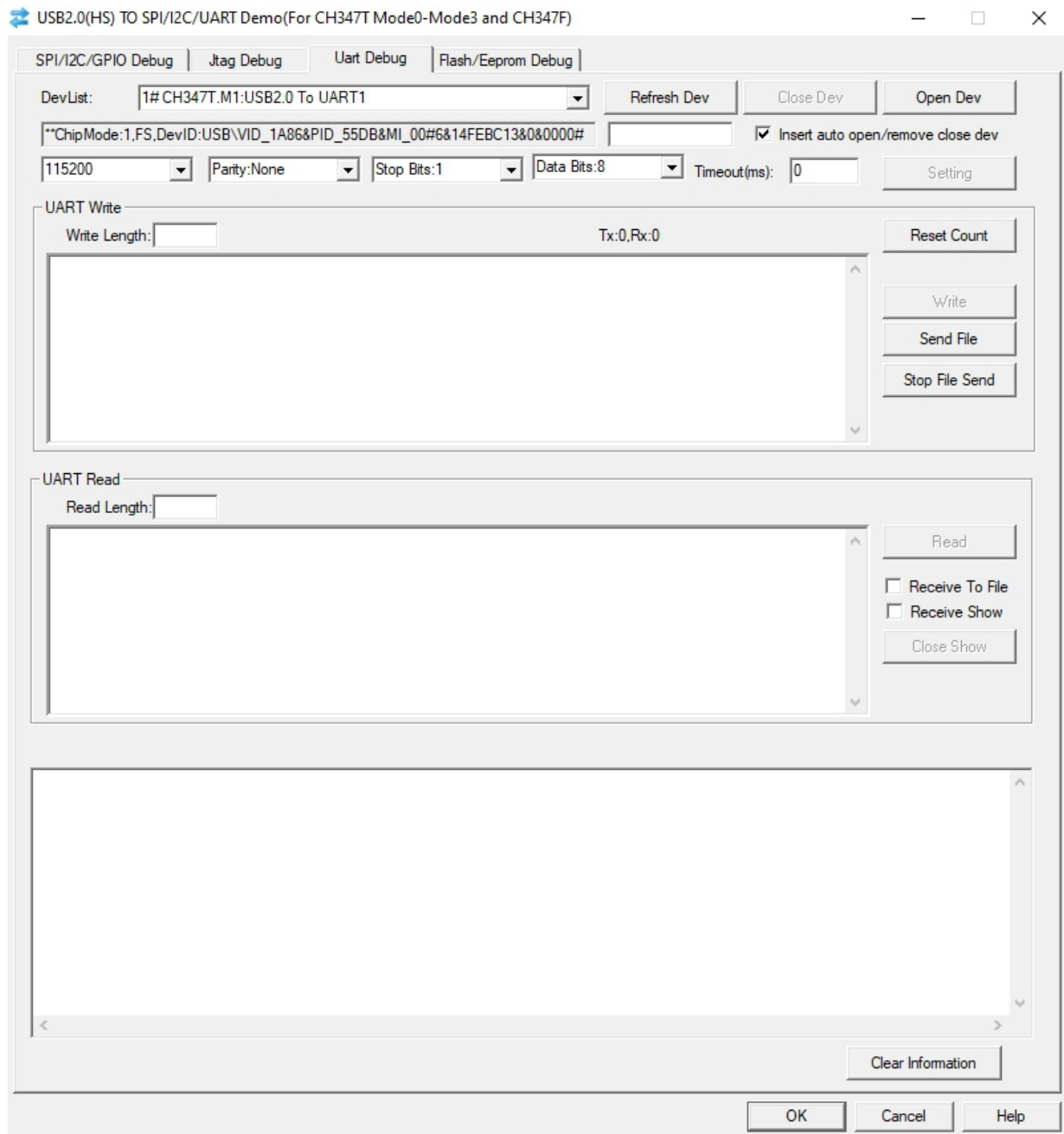
3. Function descriptions and software usage introduction

CH347Demo is a functional demonstration software used for USB to SPI, JTAG, I2C, and UART, etc. of USB2.0 high-speed converter chip CH347.

CH347Demo supports hot swap detection. The software automatically obtains and display the current working mode of CH347, supports device scan and automatic startup. You can use device event notification to obtain CH347 connection and disconnection status in real time. CH347DLL dynamic library monitors the plug and unplug of CH347 and provides library functions for searching, opening, closing, and the operation of each hardware interface. For details, see the *CH347 Application Development Manual.PDF*.

3.1. USB to UART

The CH347F and the CH347T in working mode 0 can use UART0 and UART1, and the CH347T in other working modes can use UART1. You can use the "Uart Debug" page of CH347Demo software to test UART functions.



The CH347T's VCP virtual serial port supports the use of common serial debugging tools, USB to HID serial port can directly use CH347Demo or according to the CH347DLL interface library serial port related operation functions for secondary development.

“Uart Debug” page of CH347Demo:

“Refresh Dev”: Obtain all CH347 devices on the current PC

“Open Dev”: Open CH347 device

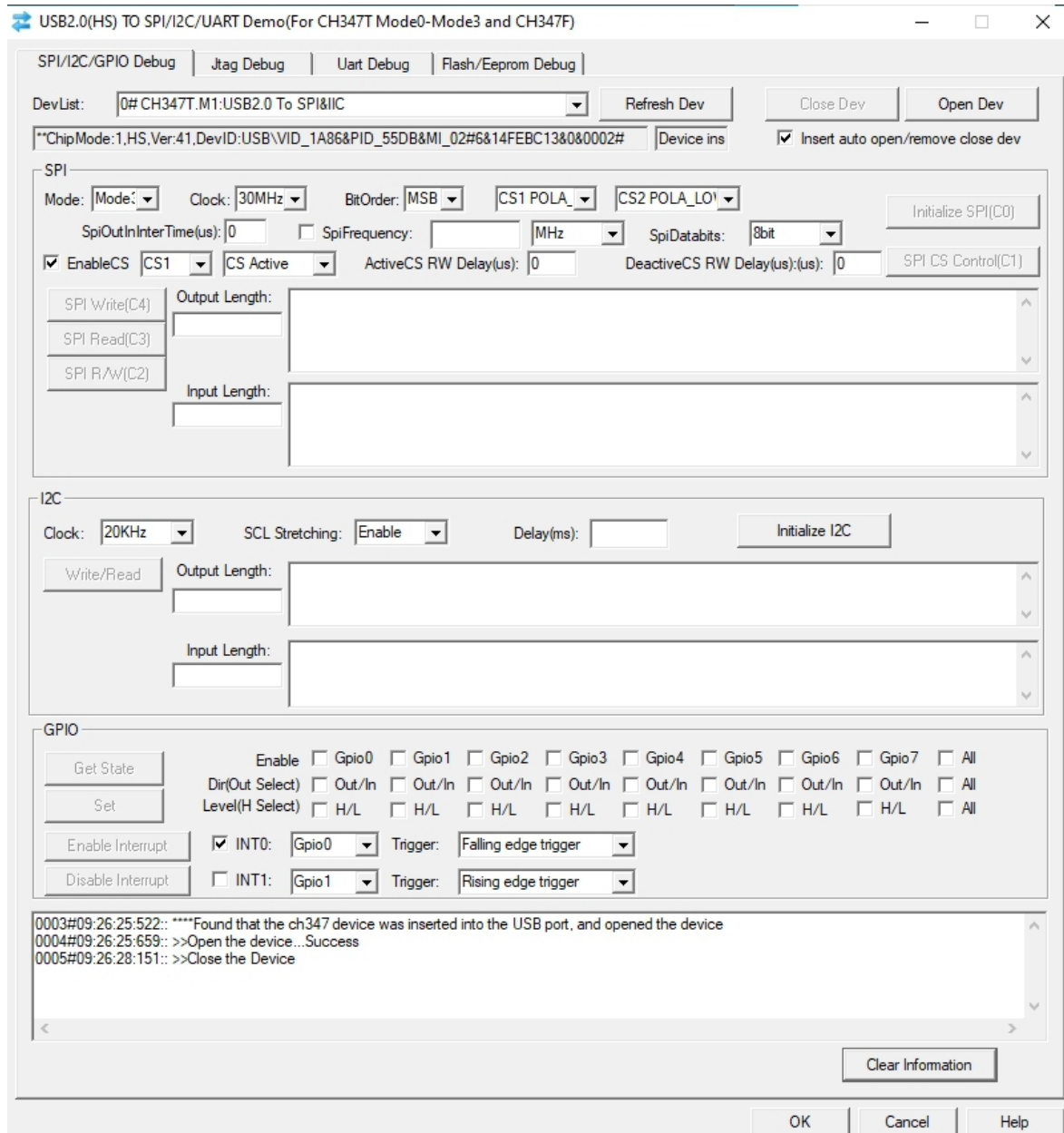
“Setting”: Setting the serial port parameters

“Receive Show”: Real-time display of data received by serial port

3.2. USB to SPI/I2C/GPIO

SPI and I2C interfaces are available for CH347F and CH347T in working mode 1/2. The CH347T evaluation

board is configured according to the P9-P14 functional pin configuration, and together with the CH347Demo, it is able to operate the peripherals connected to the SPI and I2C interfaces, or to operate the EEPROM and FLASH devices on the evaluation board. The CH347F requires no additional configuration and can operate SPI and I2C functions directly from this page.



I2C synchronous serial port of CH347F and CH347T are fully compatible with I2C bus timing and supports various I2C devices that conform to the timing, such as A/D and D/A chips, I/O expansion chips, serial memory, IC cards, and multiple devices can share the bus. In general, an I2C interface outputs several bytes first, the first byte is the device address and read/write direction, and then you can input several bytes or no bytes. The application can be designed with a speed of 20KHz, 100KHz, 400KHz, or 750KHz for 2-wire serial port, and 750KHz for the software by default.

SPI synchronization serial port of CH347F and CH347T supports SPI mode 0/1/2/3, and clock frequency up to 60MHz. Before initializing SPI, you need to confirm the SPI working mode, clock frequency, bit sequence, and CS chip select polarity supported by the SPI device.

CH347F and CH347T have a total of eight GPIOs which are silk-screened on the back of the evaluation board, and the GPIO functions can be tested through the "GPIO" operation panel after "Open Device".

“Set”: Set GPIO enable, direction, and output direction level status

“Get State”: Obtain the level status of GPIO direction and input direction

“Enable Interrupt”: GPIO pin of CH347 is a function reuse pin. You need to enable it separately before using it

“Dir (Out Select) ”: Set the selected GPIOs as outputs and leave them unchecked as inputs.

“Level (H Select) ”: Set the level state of the output direction GPIOs and gets the level state of the input direction GPIOs.

"Enable interrupt": the selected GPIO enables interrupt trigger and notification.

"Disable interrupt": the selected GPIO disables interrupt trigger and notification.

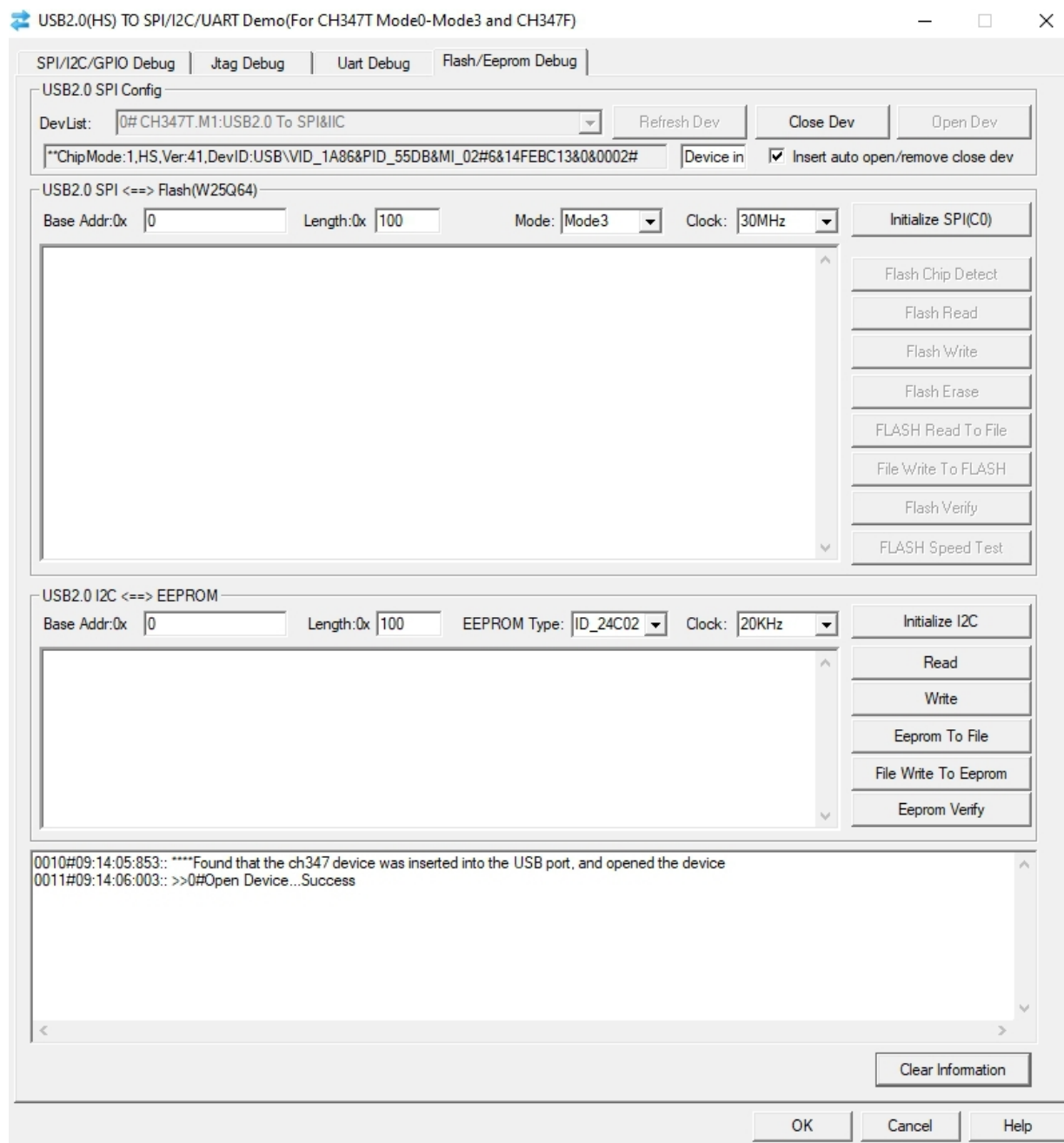
In mode 1/2, you can operate onboard EEPROM device 24C02 and FLASH device 25Q16, The CH347T evaluation board requires the pins to be configured according to the P9-P14 functional pin configuration area, and the CH347F requires no additional configuration. Users can also replace it with other models as needed.

“FLASH/EEPROM Debug” page provides common operations on EEPROM and FLASH. Default I2C communication rate is 750KHz. After selecting an EEPROM model, you can read and write EEPROM content, write files to EEPROM, or read EEPROM content and save it to a file, etc.

FLASH can be operated in Mode 0 or 3. Clock supports 60MHz, 30MHz, 15MHz, 7.5MHz, 3.75MHz, 1.875MHz, 937.5KHz, and 468.75KHz, Click "Initialize SPI(C0)" to complete the initialization of SPI interface, then FLASH device model can be automatically identified, read and write content, write files to FLASH or save FLASH content to files after reading, and test speed, etc.

“FLASH Verify”: Verifies whether FLASH data matches the selected target file.

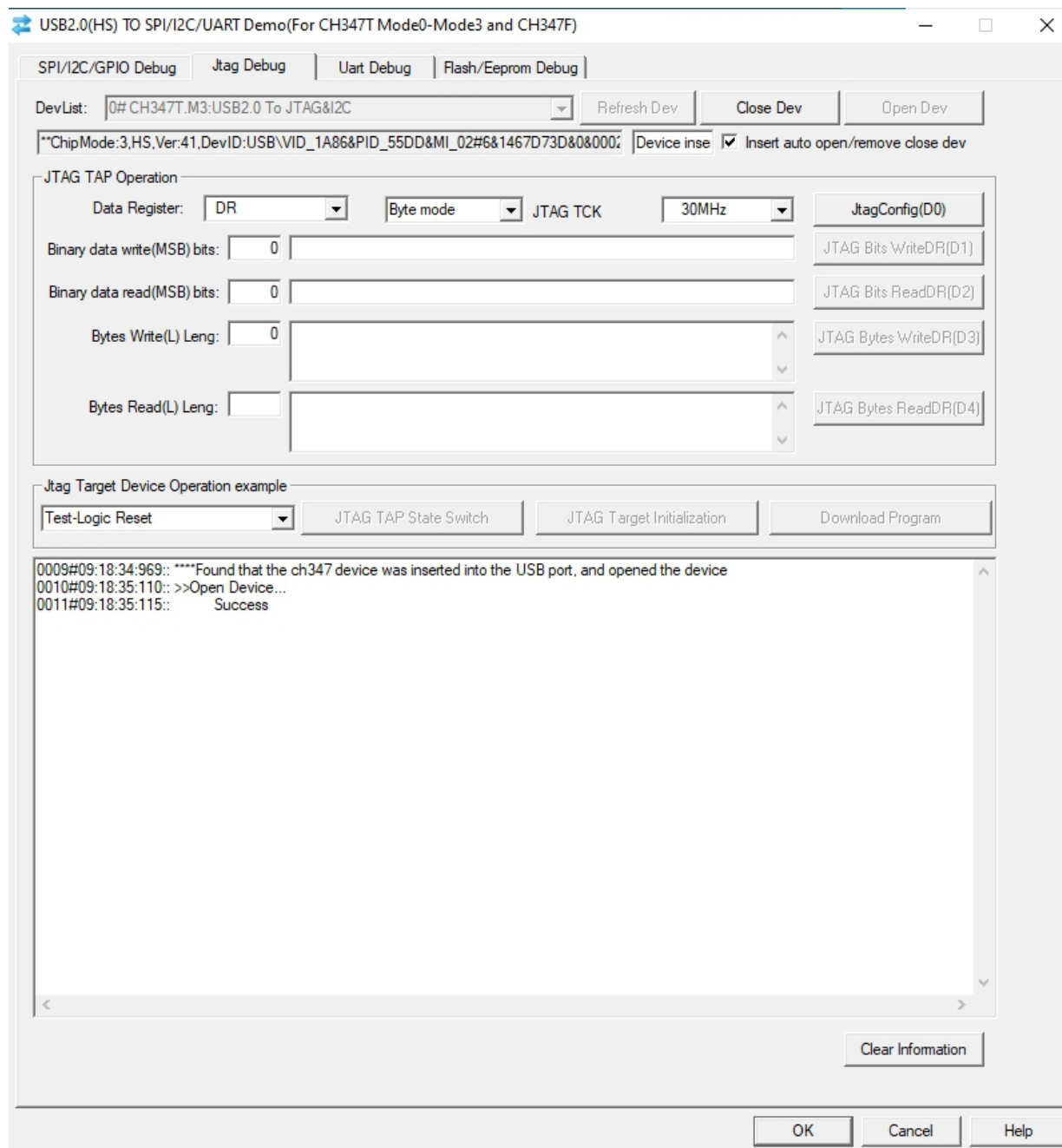
“FLASH Speed Test”: After the target file is written into FLASH, read and verify the contents, and display FLASH read, write and erase speed of this process in the information output area.



3.3. USB to JTAG

CH347 supports USB to 5-wire JTAG port, use the "Jtag Debug" page to test the JTAG function, "Open dev", then select the JTAG clock frequency and click "JtagConfig(D0)" to complete the JTAG configuration.

Select "Data Register" to switch Target board to Shift-DR/Shift-IR for read/write. You can select "Byte mode" or "Bit mode" for read/write, when you switch to Shift-IR, you can input command data in Bit mode. When you switch to Shift-DR, you can read or write command data in batches in Byte mode.



“JTAG TAP State Switch”: JTAG status switch, supports the conversion from Run-Test /Idle state to Shift-DR/Shift-IR state and then to Run-Test /Idle state.

“JTAG Target Initialization”: Switch the current Target state back to Test-Logic-Reset.

“Download Program”: After the Target state is switched to Shift-DR, data is written in bulk to simulate program download. This function is only used to test the batch read/write speed of JTAG interface in Shift-DR state, but not a real program download function.